

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 7,087,493

APPLICATION NO.: 09/921,394

ISSUE DATE : Aug. 8, 2006

INVENTOR(S) : Sudhir K. Madan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 19, Line 61 change "output of the second inverter is coupled to the second source/drain region" to -- output of the second inverter is coupled to the first source/drain region --

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 7,087,493

Date of Issue: Aug. 8, 2006

Patentee: Sudhir K. Madan

Docket: TI-30841

Title of Invention: MEMORY WITH 6T SMALL ASPECT RATIO CELLS HAVING
METAL_1 ELEMENTS PHYSICALLY CONNECTED TO METAL_0
ELEMENTS

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANTS'
MISTAKE (37 C.F.R. §1.323)**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Attn: Certificate of Correction Branch of the
Patent Issue Division

Dear Sir:

1. Issuance of a Certificate of Correction to this patent under 35 USC §255, as attached in duplicate in Form PTO/SB/44, is respectfully requested.
2. Patentees respectfully submit that a mistake appears in this patent of a minor character, as more fully described below. The error occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or require re-examination. A certificate of correction is respectfully requested.

3. The error occurs in the patent in claim 1, column 19, lines 61-63. The language “wherein the output of the second inverter is coupled to the **second** source/drain region of the second drive transistor” should read – wherein the output of the second inverter is coupled to the **first** source/drain region of the second transistor --. This error is made evident by the description in the BRIEF SUMMARY OF THE INVENTION and also from a comparison of this claim to Figures 5a, 6 and 7b.

4. As is clearly described in the BRIEF SUMMARY OF THE INVENTION in column 2, lines 19-21, “[t]he output of the second inverter is coupled to the **first** source/drain region of the second drive transistor.” (*emphasis added*)

5. Also, with reference to Figures 5a, 6 and 7b, it is readily apparent that the output of the second inverter is formed by coupling one of the source/drain regions of the second drive transistor (DT2(D)) and one of the source/drain regions of the second pull-up transistor (PT2(D)) . This is accomplished by using Metal 0 plugs 130₁₂ and 130₅ and Metal 1 conductor 132₁₀. These Figures are also described in detail in the specification in Columns 13-15. Claim 1 describes this connectivity by requiring, in Column 20, Lines 23-26, “a third conducting plug coupled to the **first** source/drain region of the second drive transistor; and a fourth conducting plug coupled to the first source/drain region of the second pull-up transistor” (*emphasis added*) and in Column 20, Lines 36-39, “a second conducting element coupled to and physically contacting the third conducting plug and coupled to and physically contacting the fourth conducting plug.” As is readily apparent, the third conducting plug must be coupled to the output source/drain of the second drive transistor and the fourth conducting plug must be coupled to the output source/drain of the second pull-up transistor and the second conducting element must couple these plugs together thereby forming the inverter output. Thus, the output of the second inverter must be coupled to the first source/drain region of the second drive transistor (and NOT the second source/drain region) since this is the source/drain region that is coupled to the third conducting plug. If the output of the second inverter were coupled to the second source/drain region of the second drive transistor, as currently claimed,

then the third conducting plug would not be coupled to the output side of that drive transistor which is clearly erroneous and would simply not form an inverter.

6. In summary, the Patentee made a simple error by using the term “second” instead of “first” in the indicated location of the claim, and this error is readily apparent from the record as described above. According to the policy of the Patent and Trademark Office, as set forth in MPEP §1481, Patentee respectfully submits that the issuance of a Certificate of Correction is appropriate in this situation.

7. The Patent and Trademark Office is requested to contact the undersigned by telephone if questions are presented by this Request, or if otherwise useful to expedite the correction of this patent.

8. Please send the Certificate to:

Name: Texas Instruments Incorporated

Address: P.O. Box 655474, MS 3999
Dallas, TX 75265

9. Please charge all required fees to charge Deposit Account 20-0668.

Respectfully submitted,

Texas Instruments Incorporated
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Dallas, Texas 75265
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/Frank D. Cimino/
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Reg. No. 52,458